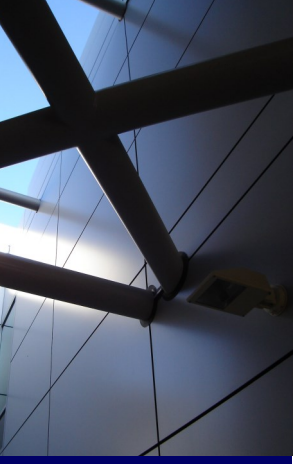

MECHANICAL ENGINEERING
DISSERTATION DEFENSE

The Department of Mechanical Engineering presents:

The Ph.D. Dissertation Defense of

Sainan Lu

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Optimization of the Thermal Performance of Three-Dimensional Integrated Circuits (3D ICs) by Utilizing the Rectangular-Shaped and Disk-Shaped Heat pipes and the Integrated Chip-Sized Double-Layer and Multi-Layer Microchannels

Doctor of Philosophy, Graduate Program in Mechanical Engineering
University of California, Riverside, June 2022
Dr. Kambiz Vafai, Chairperson

Moore's law has been applicable for many of the electronics advancements. The issue of coming up against proper thermal management prevents these features from being produced much smaller. Hence, the industry has moved from a two-dimensional approach to a three-dimensional setup to utilize the volume more efficiently. A three-dimensional integrated circuit (3D IC) is a metal-oxide semiconductor-integrated circuit manufactured by stacking silicon wafers or dies and interconnecting them vertically using through-silicon vias (TSVs), such that they behave as a single integrated device to achieve higher performance, lower power consumption, higher functional density, lower transistor packaging density, and a smaller form factor than conventional two-dimensional integrated circuits. Due to drastically increased integration density of 3D ICs, the tasks of removing a large amount of dispersed heat from a constrained space is beyond the capability of conventional cooling techniques.

Rectangular-shaped and disk-shaped heat pipes (RSHPs and DSHPs) and integrated chip-sized double-layer and multi-layer microchannels (DLMCs and MLMCs), as innovative heat sinks, are investigated to optimize the thermal performance of 3D ICs in this work. The results show that both RSHPs and DSHPs contribute to improve the overall thermal performance and reduce the hotspot temperature by 7K and 11K on average, respectively. Furthermore, utilizing the RSHP or DSHP as the heat spreader in place of the solid copper heat spreader further optimizes the thermal performance with the reduction of the junction temperatures 14K and 16K on average, respectively. The chip-sized integrated DLMC without a heat spreader and a heat sink reduced the hotspot temperature by almost 15 K for a nominal 3D IC structure. Meanwhile, the weight of the chip-sized integrated DLMC is 1421 times lighter and the size is significantly smaller than the copper heat sinks. Furthermore, two chip-sized integrated DLMC lowered the hotspot temperature by another 5 K compared with utilizing just one integrated DLMC on top of the chip structure. The results also show that the MLMC have a great effect on reducing the hotspot temperature. The proposed structures and results presented in this study pave the way for major innovations in resolving the thermal issues for the 3D ICs.